

Analog Front-End Circuitry for Biphasic Stimulus Signal Delivery Finding Use in Neural Stimulation

This technology uses a low voltage and modern bulk- complementary metal-oxide-semiconductor design that are highly programmable and allow experimentation with waveforms and simulation patterns for topologies.

What is the Problem?

Rapid advances in understanding brain function, neural connectivity and neural plasticity are providing opportunities to develop systems to aid the diagnosis and treatment of neurological disorders. Electrical neural stimulators are being used alongside neural recording systems to enable bidirectional interactions with the nervous system and realize new neuroprostheses and rehabilitation methods. In delivering electrical stimuli to neural tissue, biphasic, current-regulated pulses are typically applied between two electrodes using specialized electronics, with the resulting electrode-tissue-interface having a complex electrical impedance (ZE). This requires high headroom voltage and invariant impedance. Current complementary metal-oxide-semiconductor (CMOS) designs are on silicon, allowing for integration on a single silicon die. While compact, these will be limited by the headroom voltage.

What is the Solution?

A neural stimulator architecture is described which can drive biphasic, constant-current waveforms through a wide range of electrode impedances with approximately $\pm 11V$ compliance, while using a low-voltage, modern bulk-CMOS technology. These are highly programmable; these developed electronics can safely apply current signals synthesized via standard low power integrated current DAC topologies to the electrode/interface (which may sit at a high voltage). Therefore, these electronics empower researchers and clinicians, allowing them to experiment with numerous waveforms and stimulation patterns.

What is the Competitive Advantage?

Extending CMOS stimulator voltage compliance past individual device limits has been previously investigated. However, voltages exceeding VDD can be created at the driver output, potentially causing device failure, junction breakdowns, and unregulated current through ZE. While ZE should “self-discharge” if given time, it is impractical to have the system design and simulation pattern determined by an empirically found decay rate which could change over time. This system will avoid device failure and allow the clinician to experiment with numerous waveforms

Technology ID

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Category

Hardware/Semiconductors
Selection of Available
Technologies

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and stimulation patterns.

Patent Information:

[US10307594B2](#)

References

1. E. Pepin, D. Micheletti, S. Perlmutter, Jacques Rudell, Jacques Rudell(41913) ,
https://www.researchgate.net/publication/286813813_High-voltage_compliant_capacitive-load_invariant_neural_stimulation_electronics_compatible_with_standard_bulk-CMOS_integration, 2014 IEEE Biomedical Circuits and Systems Conference