

## Dual Feedback Loops for Integrated Voltage and Clock Regulation

**This technology offers an improved all-digital unified clock with power architecture to regulate a clock signal and a supply voltage in a single loop. This device allows for a more efficient operation of digital load to perform quicker computations than the existing digital systems with a first control loop and second control loop operating independently.**

### What is the Problem?

Some synchronous digital systems have a first control loop and a second control loop that operate independently. The first control loop can control a supply voltage such that the supply voltage tracks a reference voltage. The supply voltage typically powers a digital load such as a microprocessor. The second control loop controls a clock signal such that a frequency of the clock signal tracks a frequency of a reference clock signal. The clock signal is typically provided to the digital load for timing purposes. At times, the supply voltage can undesirably drift from the reference voltage. For example, a decreased supply voltage can cause the digital load to require more time to perform a given computation. Meanwhile, the clock signal frequency is typically unaffected by this change in the supply voltage. If the supply voltage decreases enough, timing errors can occur.

### What is the Solution?

Improved circuits with methods for regulating a clock signal and a supply voltage are needed. This is achieved with an all-digital unified clock and power architecture that combines switched-capacitor-based voltage control and clock frequency regulation into a single loop to significantly reduce required guardbands.

### What Differentiates it from Solutions Available Today?

Correctly operating digital SoC domains at their target frequencies require the addition of supply voltage guardbands to account for supply droop events and temperature variation. These guardbands degrade processor energy efficiency, especially in low-voltage sensor and IoT applications due to increased delay sensitivity to temperature and supply voltage variation. This method allows for a significant reduction in the required guardbands, allowing for more efficient operation of the digital load. Increased efficiency of the digital load will allow for quicker computations than existing solutions allow for.

### Technology ID

BDP 8660

### Category

Hardware/Semiconductors  
Selection of Available  
Technologies

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### Learn more



## Patent Information:

[US11277141B1](#)

## References

1. Xun Sun, Akshat Boora, Rajesh Pamula, Chi-Hsiang Huang, Diego Peña-Colaiocco, Visvesh S. Sathe(2020) , <https://ieeexplore.ieee.org/document/9162982>, IEEE Symposium