Input Driven Self-Clocked Dynamic Comparator

This technology offers a method to reduce the switching power for a dynamic comparator. It uses an input driven self-clocking mechanism instead of a constant clock that can consume less dynamic power and run faster.

What is the Problem?

What is the problem?

Ultra-low power sensor networks have been a topic of prevailing research over the last few years. These networks can be used in a wide range of applications – biomedical, security, autonomous navigation and Time of Flight Imaging. All these applications require highly power efficient Analog-to-digital converters (ADCs) to digitize the sensed signals. A key building block in virtually all converter architectures and mixed-signal electronics is a comparator, which contributes the majority of the energy consumption. For example, 50-60 % of the energy consumption in a Successive approximation register (SAR) ADC comes from the comparator. With technology scaling, this problem becomes more acute because the low voltage operation imposes stringent requirements on the quantization noise of the comparator. The most common comparator architecture used in converters is the StrongARM latch, owing to their strong positive feedback required for fast decisions, zero static power consumption, and full swing outputs. The power consumed by the latch arises primarily from the charging and discharging of the capacitances. Several methods have been proposed to reduce this switching power. Most of these techniques attempt to reduce the signal swings across the nodes.

What is the Solution?

The solution is a novel way to reduce the switching power for a dynamic comparator by using an input driven self-clocking mechanism. A dynamic comparator is operated using an external clock. Because of the switching states of the clock, there is continuous charging and discharging of the capacitance irrespective of the voltage difference at the input (VIN – VREF). But if the clock is enabled when the voltage difference is less than a certain voltage (|VIN-VREF|Δv) and disabled otherwise, the switching activity can be reduced, as shown in. This method accomplishes this using a pre-amplifier stage and a feedback loop around the comparator which causes it to oscillate. The oscillation stops when VIN>VREF on the rising edge and VIN

What is the Competitive Advantage?

Technology ID

BDP 8089

Category

Hardware/Semiconductors

Selection of Available Technologies

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Traditional analog-to-digital converters are difficult to operate at such high sampling speeds because of their high-power consumption. The main contribution to the power consumption comes from the comparator which does not scale in the same order with supply voltage and technology as for the other digital blocks. In addition to their high dynamic power dissipation, it is difficult to have a robust clock generation scheme at such a high speed. This solution is a novel self-clocked dynamic comparator architecture which can run faster and consume less dynamic power without an external clock.

Patent Information:

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